following remarks. Please charge any fees that may be incurred to the deposit account 09-0456.

**Remarks**

Claims 1-32 are pending in this application. Claims 1, 2, 4-9, 17-21, 23-27 and 29-32 are rejected under 35 U.S.C. § 102(b) as being anticipated by Morgan (U.S. Patent No. 6,083,271).

Morgan teaches an efficient method for identifying in a netlist the voltage partitioning of a design. See column 4, lines 6-15 and column 4, line 60 through column 5 line 5. Morgan is taking predetermining voltages and then organizing them so that they corresponds to voltage and ground domains and could otherwise be used to verify the design.

Applicants' invention specifies and claims how to actually achieve a functioning device using voltage islands. It describes and claims a methodology that considers timing (claims 1, 8, 15, 21 and 27) aspects; then creates and assesses the floorplan and continues to repeat such process depending on the results of the assessment (claims 1 and 15). Or unlike Morgan, Applicants' invention optimizes power consumption by appropriately using power states of logical partitions (claims 21 and 27).

In the rejection, the Examiner inferentially recognizes the limitations of Morgan. Fundamentally, the teaching of Morgan are set forth in the methodology of figure 3 which the Examiner admits only addresses how the invention takes a design and "defines" (organizes) the partitions. To address the other elements in Applicants' invention the Examiner references "vague" sections of Morgan. The first such section (col. 3, lines 38-55) provides little except to explain that once a floorplan is completed the traditional way of handling the communication between voltage groups is "manual." And this is a problem since this leads to incorrect "communications." This section is void of any explanation of the floorplan is created, assessed and then potentially

redesigned and void of any mention of how timing of power states (independent claims) are addressed.

The other section the Examiner mentions, (col. 4, lines 29-62) suffers is equally void of the claim with no teaching of the crux of what Applicants teach and claim as described above. The Examiner simply ignores the fact that what Morgan is about is a "data structure" (line 29) that "associates each group of the devices in a completed circuit design with appropriate power and ground." (lines 36-41). It is not a design system itself and there is no teaching of how "the information" created by the invention is used in the tools to provide what Applicant's invention claims.

Since Morgan really only describes how to document groupings efficiently and fails to teach the methods set forth in independent claims 1,8, 15, 21, and 27, these claims and the claims on which they depend are all allowable in the current form.

The Examiner cites some other sections of Morgan in addressing some of the dependent claims. To address the limitations in claims 2, 4 and 5 the Examiner sites the sections mentioned above as well as column 6, lines 41-63. It is clear in reading that section that this is nothing more than detailing how a designer takes a circuit design (2A) and "defines" the groupings or partitions in what appears to be an already floor-planned device. There is nothing that addresses using requirements and timing of power-states to establish voltage island; then creating a floor plan based on this set of information; assessing that floorplan and then iterating these design steps based on the original assessment. In addition there is no teaching or mention of assessing waveforms, identifying voltage ranges to comply with timing requirements as mentioned in the dependent claims.

The citation of column 2 line 22 through column 3 line 8 is clearly inapposite against claims 6 and 7. This citation seems to generally describe the fact that modern devices contain multiple voltage domains and there is a problem of keeping track of them. In any event there is no hint of "evaluating average chip power consumption . . ." (claim 6) or

"selecting from said different voltage combination that have chip timing . . ." (claim 7) in that section.

So all these dependent are for these additional reasons allowable. For the rest of the dependent claims, the Examiner cites similarities between those claims and other claims which we have already addressed. Therefore the arguments with respect to the claims referenced by the Examiner apply equally to those not addressed above.

## SUMMARY AND CONCLUSION

In conclusion, because the Examiner has failed to assert a reference that teaches the steps of the invention as claimed, Applicants have overcome Examiner's 35 USC § 102(b) rejection.

In view of the foregoing, withdrawal of the rejections and the allowance of the current pending claims are respectfully requested. If the Examiner feels that the pending claims could be allowed with minor changes, the Examiner is invited to telephone the undersigned to discuss an Examiner's Amendment.

Respectfully submitted,

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